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In this issue:

We present Part II of a technical report authored by Bruce Marler, M.S.E.E., Chief Technical Officer for WooshCom Corporation, and Mukta Kar, Ph.D., CableLabs Senior Member of Technical Staff, on an overview of MPEG-2 digital interfaces.

Baseband MPEG-2 Interfaces Part II

Editor's Note: *This article provides an overview of the main digital interfaces which exist and which are evolving for the transmission of baseband MPEG-2 transport streams. These interfaces are used in cable headends, uplink, studio, and/or transmitter facilities. For the purposes of this article, a baseband MPEG-2 interface is defined as an interface that carries raw digital bits of an MPEG-2 transport stream over an interface with only such encoding as required at the physical layer. While focusing on the physical layer of these interfaces, timing issues that complicate the conversion of one interface type to another will be highlighted.*

Some fundamental terms and concepts introduced in Part I of this article will be reviewed before providing a more detailed explanation of the DHEI, DVB-SPI, and Divicom M2P baseband MPEG-2 interfaces. Please see Part I of this article (in *Specs Technology*, Vol. 11, No. 6, October 1999) for information on the IEEE 1394, DVB-ASI, Divicom M2S, DVB-SSI, SMPTE 310M, and SMPTE 305M (SDTI) interfaces.

Review of Concepts and Terms

MPEG-2 interfaces may be categorized in different ways; some transmit serial bit streams, while others transmit parallel byte streams. An important differentiating factor in categorizing these interfaces is the relationship between the raw clock rate and the rate at which MPEG-2 data is transmitted over the interface. Two types of relationships exist between these rates:

- packet synchronous (PS), and
- packet asynchronous (PA).

In the PS case, the raw clock rate is directly proportional to the rate at which MPEG-2 data is transmitted; such interfaces contain no padding. Whereas in the PA case, the interface's raw clock rate is fixed, while MPEG-2 data is transmitted over the interface at some independently chosen rate up to some maximum allowable capacity. The capacity is determined by the raw clock rate and any overhead required by the interface. The PA interface may be thought of as a fixed-size pipe through which data may be pumped at any rate up to the maximum capacity of the pipe. The PS interface is more like a custom-sized pipe, the capacity of which has been matched to the data rate.

Another differentiating factor is the presence or absence of higher layer protocols that somehow encapsulate the MPEG-2 data packets. According to our baseband definition, interfaces with such encapsulation are not truly baseband MPEG-2 interfaces. However, because of the importance of the following two interfaces, the scope of this article has been extended to include them:

- the IEEE 1394 interface, which is emerging as the interface of choice for set-top boxes (STBs), and
- the SMPTE 305M interface, which will extend the ubiquitous SDI interface (259M) to the MPEG-2 environment.

The table on page 2 provides a brief summary of the more popular interfaces and their primary characteristics, with a more detailed description in the paragraphs which follow.

Interface Name	Type	Serial/Parallel	Max Distance (feet)	Raw Clock Rate (MHz)	MPEG-2 Data Capacity (Mbps)	PHY Layer Encoding	Electrical Levels	Connector/ Cable Type
DVB-ASI	PA	S	300	270	214	8B/10B	Fiber Channel FC-0	Coax 75Ω & multi-mode fiber
Divicom M2S	PA	S	75	270	100	8B/10B	Custom Levels	In SMA–50Ω Out SMB–50Ω
DVB-SSI	PS	S	450 for coax	<105	Same as clock rate[1]	Biphase Mark	Custom see EN 50083-9	Coax 75Ω & Fiber-optic
SMPTE 310M	PS	S	300	19.39 & 38.78	Same as clock rate	Biphase Mark	AC-coupled ECL	Coax–75Ω
SMPTE 305M (SDTI)	PA	S	984	270 360	200–225 270–300	Scrambled SMPTE 259M	Fiber Channel FC-0	Coax–75Ω Fiber-optic
DHEI	PS	S	16 12	29 & 39	Same as clock rate[1]	None	Diff ECL	Simplex 15 Pin HD-22 Duplex 26 Pin HD-22
SWIF	PA	S	33	54	52.3	Scrambled & Layered	660 nM	Fiber-optic–HP Versatile Link
DVB-SPI	PS	P	unknown	<13.5	108	None	LVDS	25 Pin D type
Divicom M2P	PS	P	30	0.5–12.5	8*Clock Rate[2]	None	RS-422	25 Pin subD
IEEE 1394	PA	S	13.5	98.304 196.608 393.216	Unknown	Only Data-strobe	Custom Diff Low Voltage	4- or 6-pin IEEE1394 110Ω Twisted Pair

[1] Same as clock rate unless forward error correction (FEC) or FEC gap is present where FEC bytes were present. In the latter case, the maximum capacity would be 188/204 times the raw clock rate of the interface.

[2] The data rate can be lower than 8*Clock Rate if there is an inter-packet gap for optional error correction codes. This inter-packet gap is programmable and can be from 0 to 255 bytes long.

DHEI (Day-Hee)

The DigiCable Headend Expansion Interface (DHEI) is intended for the transport of MPEG-2 system multiplexes between pieces of equipment in the headend. It originally was a proprietary interface of General Instrument, but now has been standardized by the SCTE (Society of Cable Telecommunications Engineers) for use in the cable industry.

It has two variations: simplex and duplex. The simplex version supports a unidirectional point-to-point link between pieces of headend equipment. Whereas, the duplex version supports a full simultaneous bi-directional synchronous link. The duplex interface is supported by GI's

integrated receiver transcoders (IRT 1000/2000), and is used to allow expansion of the number of multiplexes that can be processed. In such an expansion scenario, the DHEI expansion-out connector on the base unit is connected to the DHEI expansion-in connector on a supporting IRT (further units can be chained in a similar fashion to the supporting IRT). The interface allows the transport stream multiplex to be transmitted synchronously to the supporting unit, where additional program streams can be decrypted and encrypted and sent back to the base unit. Each IRT can process 12 services, and therefore the overall capacity can be increased in increments of 12 by the chaining of additional IRTs via the DHEI ports.

The simplex version is designed more for simple point-to-point interconnects, where no chaining is required. An example would be the connection of an IRT receiving a satellite signal, to GI's new modular processing system (MPS), where a duplex DHEI connector is connected to a simplex DHEI input on the MPS by means of a special cable. The MPS receives, processes, and internally modulates (via QAM) the transport stream. Because the stream is never returned to the IRT, a duplex connection is not required. Another example might be the connection of a video-on-demand (VOD) server to the encryption side of an IRT (again using a special cable), or connections to and from a re-multiplexer at the headend to change the program lineup. The popularity of the simplex DHEI interface is increasing as it is being incorporated on more and more pieces of third-party equipment.

The maximum specified length of the DHEI cable is less than 16 feet for clock rates below 30 MHz, and 12 feet for clock rates less than 40 MHz (although the cables that GI sells do not exceed 2 meters). DHEI is a point-to-point synchronous serial interface, which uses 3-row, D-type multi-pin connectors and differential ECL signal levels. The data, clock, and synchronization signals use balanced differential controlled impedance (120Ω) lines. The simplex version uses a 15-pin, DB-9 HD-22 connector, while the duplex version uses a 26-pin, DB-15 HD-22 connector. A reference clock and a packet clock are present on the interface. The continuous reference clock can be used to drive a piece of equipment's internal clock. The packet clock is synchronous with the data and is gapped, which means that there are missing pulses in the signal area where FEC block codes and framing bits are present. The packet clock gap can be fixed at 16 bytes, or it can vary between 46 bytes and 47 bytes when used with an IRT 2000 that is processing the I or Q side of a split-multiplex.

DVB-SPI

The SPI interface is a fairly popular point-to-point unidirectional parallel interface for connecting infrastructure equipment at the headend or within an uplink site. Since the transport packet rate is locked to the clock rate, the interface is PS; it transmits byte wide with a clock, packet sync, and data-valid signal. The data-valid signal is used to differentiate between bytes that are part of the 188/204 byte packet versus dummy bytes that follow a 188-byte packet.

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The clock rate is not fixed, but rather varies with the rate of the transport stream to be transmitted. However, it is limited to 13.5 MHz, which corresponds to a maximum bit rate of 108 Mbps.

The physical connector used on equipment is a 25-pin, D-type female. Electrically balanced differential LVDS NRZ signals are employed with 100Ω destination termination. The specification does not define the interconnecting cable in any way, but it would be wise to employ, at a minimum, a twisted-pair cable with as close to a 100Ω characteristic impedance as possible; a 100Ω source impedance would help further. In a parallel interface, both cable attenuation and signal skew impair correct reception of the signal. Because of this, and because so much freedom is given in cable selection, it is impossible to predict a maximum cable length.

Divicom M2P

This is a proprietary parallel interface developed by Divicom before a standard existed for transmitting MPEG-2 streams. It is very similar to the DVB-SPI, except for the existence of an external clock input signal, a different pinout, different electrical levels, and different usage of the data valid signal. It is a purely PS interface with a variable-byte clock rate that is proportional to the stream's data rate up to a maximum frequency of 12.5 MHz.

The data-valid signal is asserted to the valid state during the 188-byte packet time and is de-asserted during the inter-packet gap. For M2P, the inter-packet gap may be any length up to 255 bytes. This inter-packet gap may be used for a Reed-Solomon error correction code. M2P also has an additional signal, INCLK, which is used as an external frequency source for use in cases where a modulator needs to drive a clock to an encoder or remultiplexer, which is sourcing the transport stream. Electrically, the interface uses 100Ω balanced differential lines with RS-422 signal levels, and a 100Ω source and destination termination. The cable is a shielded, twisted-pair cable of 24 conductors with a maximum length of 30 feet.

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